Abstract Of The Disclosure

A clocking circuit includes primary and secondary clock sources. These sources are input to a multiplexer which selectively chooses between them. A PLL stabilizes the output of the multiplexer. A clock detection circuit monitors the presence of the primary clock source and drives the multiplexer such that if the primary clock source fails, the backup clock is selected. Also upon clock switchover, a feedforward correction circuitry modifies a time constant within the PLL to mitigate clock skew during switchover.